(12) UK Patent Application (19) GB (11) 2 165 410 A

(43) Application published 9 Apr 1986

(21) Application No 8522013

(22) Date of filing 4 Sep 1985

(30) Priority data

(31) 8422732 (32) 8 Sep 1984 (33) GB

(51) INT CL⁴
G11C 11/40 H03K 17/24

(52) Domestic classification
H3T 2B2 2B3 2T3F 2T3X 2T4 3J 4D 4S 5E G
H1K 11A3 11C4 11D1 11D 1CA 4C14 4C1C GAF

(56) Documents cited
None

(58) Field of search
H3T

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(54) Memory cells

(57) A memory cell, for use in an integrated circuit device, comprises two cross-coupled inverters. Each inverter comprises a pair of MOS transistors T1, T2 and T3, T4 (6, 8 Fig. 2) having a diffused control electrode C1, C2 (14) and a floating gate FG1, FG2 (12) arranged so that it is common to both MOS transistors (6, 8). The cell enables volatile and/or non volatile storage of data with differential sensing of non volatile data stored on the floating gates. Data is stored in non-volatile form by raising V_{DD} to a high level so that tunnelling can occur at tunnelling regions TR1, TR2, thereby transferring charge to or from the floating gates via control electrodes C1, C2 and nodes N1, N2.

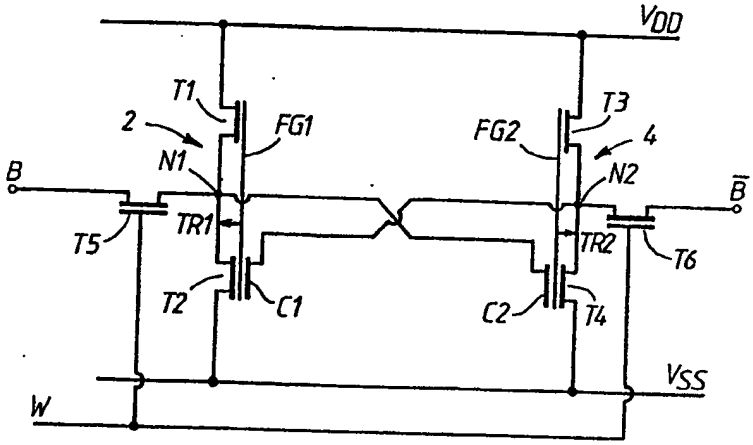

FIG. 1.

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The drawing originally filed was informal and the print here reproduced is taken from a later filed formal copy.

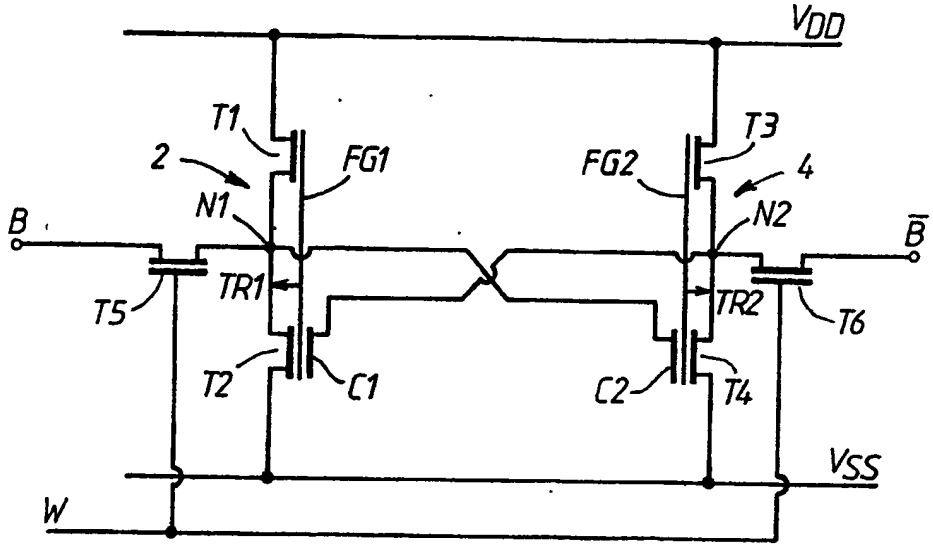

FIG. 1.

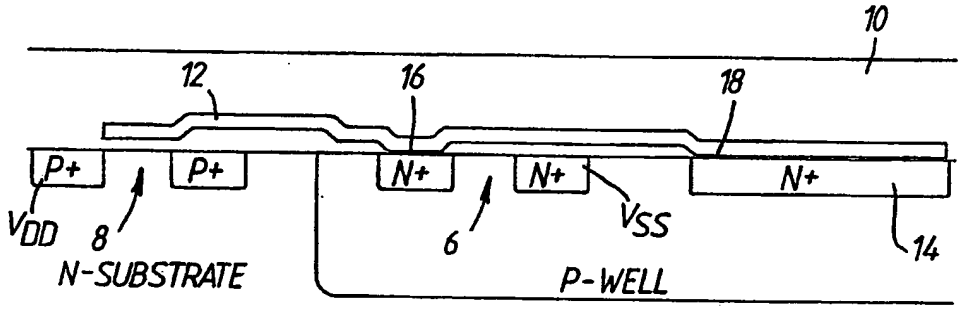

FIG. 2.

SPECIFICATION

Memory cells

The present invention relates to memory cells.

Generally, memory cells may be divided into two main groups; namely, volatile memory cells and non volatile memory cells.

Volatile memory cells employ logic elements to store data which can be continously updated from an exterior data source. This type of memory cell is termed 'volatile' as the data stored is lost if there is an interruption in the supply voltage to the device. One type of volatile memory is a Random Access Memory (RAM).

Non-volatile memory cells also utilise logic elements to store data but, with certain types of non-volatile memories it is not possible to update the stored data as the logic states of the memory cells are determined by the physical construction of the logic elements themselves. Cells of this type are termed 'non-volatile' as the data stored in the cell is not lost if there is an interruption in the supply voltage to the device. One type of non-volatile memory is known as a Read Only Memory (ROM).

Another type of non-volatile memory is an Electrically Erasable Read Only Memory (EEPROM). In this device the basic memory cell usually comprises a Metal Oxide Silicon (MOS) transistor which is provided with two gate electrodes. One gate electrode consists of a conventional gate electrode known as the control gate, which in the manufacture of the device is arranged to overlie the second gate. The second gate is contained within and entirely surrounded by the oxide layer of the MOS transistor and is known as a floating gate as, when the device is in use, the second gate is not directly connected to any source of electrical potential. The floating gate is fabricated such that a portion thereof is separated from the semiconductor regions of the device by a very thin section of the oxide layer.

This very thin section of the oxide layer is known as the tunneling oxide region as, when a voltage exceeding a predetermined value appears across the thin section of the oxide layer, a charge transfer occurs between the semiconductor regions and the floating gate thereby establishing a charge on the floating gate. The floating gate is fabricated from a conductive material, such as metal or polysilicon, and hence, any charge transferred through the tunneling oxide region dissipates quickly over the floating gate. As the floating gate is surrounded by the oxide layer, which normally consists of silicon dioxide an excellent insulator, the charges transferred to the floating gate may, unless removed, remain for several years.

It can be seen, therefore, that data can be read into the cell and stored on such floating gates. As the data remains on the floating gate independently of the voltage supply to the device, the cell acts as a non-volatile memory into which data can be programmed from an external data source.

It has previously been proposed to incorporate such floating gates into volatile random access memories (RAMs) to produce memories which are able to function both as volatile and non-volatile memories. In such memories volatile information can be updated without disturbing the non-volatile stored date, which can be recalled by appropriate interrogation of the cell.

However, the tunneling oxide region usually comprises an extremely thin section of oxide, typically 20 to 100Å. In order to maintain the charge stored on the floating gate it is essential that the tunneling oxide region is free from defects such as pinholes, as these defects can provide a leakage path for the charge stored on the floating gate, with subsequent loss of the stored data. To minimise the probability of such defects during manufacture of the memories it has been found beneficial to reduce the area of the tunneling oxide region to a minimum.

However, the magnitude and duration of the applied voltage which is required to induce charge transfer to the floating gate is dependent upon several factors, including the capacitive coupling between the drain region and the floating electrode of the MOS transistor, and also the capacitive coupling between the control electrode and the floating gate.

As previously stated, it is common to fabricate such cells with the control electrode overlying the floating gate and cells of this type usually require a relatively large voltage pulse, typically 20 volts, to induce tunneling to the floating gate.

The control electrode may be a diffusion within the semiconductor substrate, formed so that it overlies and is spaced from the diffused control electrode by a thin region of the oxide layer in a manner similar to the tunneling oxide region. If the area of the diffused control electrode is made relatively large, the capacitive coupling produced between the floating gate and the control electrode is relatively large.

Furthermore, the capactive coupling between the floating gate and the diffused control electrode is large in comparison to the capacitance between the floating gate and the semiconductor layers at the tunneling oxide region such that the charge transfer to the floating gate at the tunneling oxide region is not adversely affected.

It is an aim of the present invention to provide an improved memory cell having a diffused control electrode and both volatile and non-volatile modes of operation.

According to the present invention there is provided a memory cell for volatile and/or non volatile storage of data, the memory cell comprising two inverters, each inverter having a pair of complementary metal oxide silicon transistors, wherein each inverter has a diffused control electrode, and a floating gate common to the complementary transistors of the inverter, the inverters being cross coupled with the node between the complementary transistors of each inverter coupled to the control electrode of the other inverter, whereby differential sensing of non volatile data on the floating gates of the inverters may be achieved.

Each floating gate may be formed from

polysilicon.

The present invention will now be described, by way of example, with reference to the accompanying drawings in which:

Figure 1 illustrates a schematic diagram of a memory cell in accordance with the present invention; and,

Figure 2 is a schematic cross sectional view of an inverter of the memory cell illustrated in Figure 1.

Referring to figure 1, a memory cell comprises two inverters 2 and 4 which are cross coupled to operate as a bistable latch circuit. The inverters 2, 4 comprise, respectively, pairs of complementary metal oxide silicon (CMOS) transistors T1, T2 and T3, T4, series connected at nodes N1 and N2 across voltage supplies VSS and VDD. The complementary pairs of CMOS transistors T1, T2 and T3, T4 have, respectively, common floating gates FG1 and FG2 and diffused control electrodes C1 and C2. The control electrodes C1 and C2 are diffused into the semiconductor layers of the MOS transistors and are separated from the floating gates FG1 and FG2 by a thin layer of oxide, as shown in Figure 2.

Charge transfer to the floating gates FG1 and FG2 takes place, respectively, through tunneling oxide regions TR1 and TR2.

The inverters 2, 4 are cross coupled by connecting the control electrode of one inverter to the node of the other inverter, as shown in Figure 1. The nodes N1 and N2 are also connected respectively to true and inverse bit lines B and $\overline{B}$ (B bar) via access transistors T5 and T6, and to a common word line W.

The construction of the CMOS transistors of the inverters 2, 4 can be seen in Figure 2. Each inverter comprises an N-channel transistor 6 and P-channel transistor 8. An insulating oxide layer 10 overlies the semiconductor layers and a floating gate 12 is formed within the totally encased by the insulating oxide layer 10. A diffused control electrode 14 is formed in the semiconductor layer of the N-channel transistor 6. The floating gate 12 is formed in the oxide layer 10 such that it extends very close to the underlying semiconductor layer to form a tunneling oxide region 16 through which charge transfer to the floating gate 12 can occur. The floating gate 12 also extends very close to the surface of the diffused control electrode 14. The floating gate 12 is formed in this way to produce a region 18 where there is relatively high capacitive coupling between the floating gate 12 and the control electrode 14. This relatively high capacitive coupling is sufficient to enable a charge transfer to the floating gate 12 to occur through the tunneling region 16 when the supply voltage VDD is above approximately 10 volts.

The memory cell shown in Figure 1 has the following modes of operation

(i) Volatile data storage
(ii) Non-volatile data storage
(iii) Non-volatile data retention
(iv) Non-volatile data recall.

For volatile data storage, the cell behaves as a normal CMOS static RAM cell. In this mode of operation data can be written into and read from the cell via the access transistors T5 AND T6 and the bit lines B and $\overline{B}$. In this mode of operation the voltage supplies are, typically, VSS = OV and VDD = +5V.

Data can be written into the cell by holding the bit lines B and $\overline{B}$ in the appropriate condition by, for example, applying the voltages VSS and VDD to these lines, and, at the same time, driving the word line W high to enable the access transistors T5 and T6. When the access transistors T5 and T6 are enabled the cell latch acquires a state as determined by the condition of the bit lines B and $\overline{B}$. The word line W is then driven low to disable the access transistors T5 and T6 and isolate the cell from the bit lines B and $\overline{B}$.

Data can be recalled from the cell by enabling the access transistors T5 and T6 by driving the word line W high. The data stored in the cell, represented by voltage levels at the nodes N1 and N2, appears on the bit lines B and $\overline{B}$ and may be detected by sense amplifiers (not shown). However, as the cell is operating as a volatile RAM cell the stored data will be lost if there is an interuption in the voltage supplies VSS and VDD.

The cell shown in Figure 1 may also operate in a non-volatile data storage mode. In this mode of operation data is stored as non-volatile data by inducing a charge differential on the floating gates FG1 and FG2. Initially, the supply voltages VSS and VDD are held, respectively, at OV and +5V and data is written in to the cell in the manner previously described with respect to volatile data storage.

The non volatile data storage mode can be seen by the following example. Assume that the data written into the cell in the volatile data storage mode causes the node N1 to go high (near to the supply voltage VDD) and the node N2 to go low (near to the supply voltage VSS). Node N1 is connected directly to the control electrode C2 of the inverter 4 and hence, as the node N1 is high, the control electrode C2 is also high and the transistor T4 will conduct. Likewise, as the node N2 is low, the control electrode C1 of the inverter 2 is low and transistor T2 will be held OFF. At this stage, the data is stored in the cell as volatile data by the states of the latches of the memory cell. If the supply voltage VDD is now raised from +5V to a write voltage VR, such as +15V, the voltage at the node N1 will rise to almost +15V. As the control electrode C1 is low (almost OV as it is connected to the node N2) the floating gate FG1 will also be low. Hence, almost the entire write voltage VR of +15V will appear across the tunneling oxide region TR1 of the inverter 2, with the node N1 positive with respect to the floating gate FG1. The write voltage VR appearing across the tunneling oxide region TR1 is sufficient to induce tunneling in the region TR1 and hence, a positive charge is transferred to floating gate FG1 of the inverter 2.

The node N2 of inverter 4 is low at almost OV and, since the node N1 is high, the control electrode C2 is also high. Thus, transistor T4 is held ON and transistor T3 is held OFF. As the supply voltage VDD is raised to the write voltage VR, that is from +5V to +15V, the node N2 remains near to OV but the control electrode C2 and thus the floating gate FG2 rise to almost the write voltage VR (+15V) as the

control electrode C2 is connected to the node N1. Therefore, almost the whole of the write voltage VR of +15V also appears across the tunneling oxide region TR2 of the inverter 4 with the node N2 negative with respect to the floating gate FG2. This voltage across the tunneling oxide region TR2 is sufficient to induce tunneling in the region TR2 and hence, a negative charge is trnsferred to the floating gate FG2. It can be seen that the voltages appearing across the tunneling oxide regions TR1 and TR2 are of substantially equal but opposite polarity. If the tunneling oxide regions TR1 and TR2 have substantially equal charge transfer efficiences, the charges stored on the floating gates FG1 and FG2 will be of opposite polarity but substantially equal in magnitude, thereby producing symmetrical threshold voltage shifts on each side of the latch. By storing complementary data in each side of the memory cell latch, differential sensing during recall of non volatile stored data, as described subsequently, enables the cell to distinguish very small stored charge inequalities, thereby enhancing the endurance and retention capabilities of the cell. As the charges are retained on the floating gates FG1 and FG2 the data written in to the cell is stored as non-volatile data. Furthermore, non-volatile data stored as charges on the floating gates FG1 and FG2 is retained during subsequent operation of the memory cell in the volatile data retention mode previously described.

When it is required to use the cell in the volatile data storage mode whilst non-volatile data is retained on the floating gates FG1 and FG2, the supply voltage VSS is retained at OV and the supply voltage VDD is reduced from the write voltage VR at +15V to its initial level of +5V. Volatile data can now be written into or recalled from the cell by enabling the access transistors T5 and T6, as previously described. During this mode of operation, the maximum potential which can appear across the tunneling oxide regions TR1 and TR2 is VDD which at +5V is insufficient voltage to induce tunneling in the tunneling oxide regions TR1 and TR2. Hence, the charges on the floating gates FG1 and FG2 representing the non-volatile data are maintained during the volatile data storage mode of operation.

When the supply voltages are interrupted the voltages VDD and VSS are at OV. The only potentials within the cell are the low voltage charges stored on the floating gates FG1 and FG2 resulting from non-volatile storage of data. These voltages are far below the voltages required to induce tunneling in the tunneling oxide regions TR1 and TR2 and consequently, charge leakage from the floating gates FG1 and FG2 is extremely low as they are contained within the oxide layer, an extremely good electrically insulating material.

To recall stored non-volatile data the supply voltages VDD and VSS are restored to the memory cell. The non-volatile data stored as charge differentials at the floating gates FG1 and FG2 will have the effect of either repelling or attracting electrons from the surface of the semiconductor substrate in the channel region of the MOS transistors, depending upon the polarity of the charge on each floating gate. For example, assume the example described previously with respect to non-volatile data storage with the floating gate FG1 storing a positive charge and the floating gate FG2 storing a negative charge.

As floating gate FG1 stores a positive charge the threshold voltages of the transistors T1 and T2 are shifted negative with transistor T1, being a P-channel device, having a higher threshold voltage than transistor T2, an N-channel device. The floating gate FG2 stores a negative charge and hence, the threshold voltages of transistors T3 and T4 are shifted positive, with transistor T3, being a P-channel device having a lower threshold voltage than transistor T4, an N-channel device.

As the supply voltage VDD rises towards +5V transistor T3 will start to conduct before transistor T1 since its threshold voltage is lower than that of transistor T1. Consequently the voltage at the node N2 will rise faster than the voltage at the node N1 tending to switch on transistor T2 before transistor T4 as the node N2 is connected to the control electrode of transistor T2; a situation which is enhanced by transistor T2 having a lower threshold voltage than transistor T4. This imbalance results in the memory cell acquiring a stable state with the node N2 high at almost the supply voltage VDD and the node N1 low at almost the supply voltage VSS, which is the inverse of the originally stored data.

The recalled non-volatile data at the nodes N1 and N2 can be read by enabling the access transistors T5 and T6 and can be reverted to its true state by passing through an inverter (not shown).

It can be seen, therefore, that a memory cell in accordance with the present invention provides volatile and non volatile modes of storage but is simple in operation; requiring no additional control lines when compared to conventional volatile static RAM cells. Furthermore, the cell is simple in configuration and hence can be fabricated in an integrated circuit device in an area which is only marginally larger thanb a conventional volatile CMOS RAM cell.

Although the present invention has been described with reference to a particular embodiment it is to be understood that modifications can be effected within the scope of the invention.

CLAIMS

1. A memory cell for volatile and/or non volatile storage of data, the memory cell comprising two inverters, each inverter having a pair of complementary metal oxide silicon transistors, wherein each inverter has a diffused control electrode, and a floating gate common to the complementary transistors of the inverter, the inverters being cross coupled with the node between the complementary transistors of each inverter coupled to the control electrode of the other inverter, whereby differential sensing of non volatile data on the floating gates of the inverters may be achieved.

2. A memory cell according to claim 1 wherein, for each inverter, the control electrode is diffused

within a semiconductor layer and the floating gate is arranged within an oxide layer so that it extends to overlie the control electrode and the transistors, but is separated therefrom by tunneling regions of the oxide layer which are dimensioned to permit charge transfer therethrough, and wherein the control electrode and the floating gate are arranged such that the capacitive coupling therebetween is relatively large in comparison to the capacitive coupling between the floating gate and the drain regions of the transistors.

3. A memory cell according to claim 2 wherein the capacitive coupling between the floating gate and the control electrode, and the floating gate and the drain regions are arranged such that charge transfer to the floating gate, to enable non volatile storage of data, can occur when a voltage exceeding approximately 10V is applied to the memory cell.

4. A memory cell according to claim 2 or claim 3 wherein the tunneling regions have a thickness in the range of 20 to 100 A.

5. A memory cell according to any one of the preceding claims wherein the floating gate comprises polysilicon.

6. A memory cell according to any one of the preceding claims comprising, for each inverter, a bit line, for affording data to the inverter, and an access transistor for coupling the bit line to the node between the complementary transistors of the inverter.

7. A memory cell substantially as hereinbefore described with reference to the accompanying drawings.

8. An integrated circuit device comprising an interconnected array of memory cells according to any one of the preceding claims.

Printed for Her Majesty's Stationery Office by Courier Press, Leamington Spa. 4/1986. Demand No. 8817356.
Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.